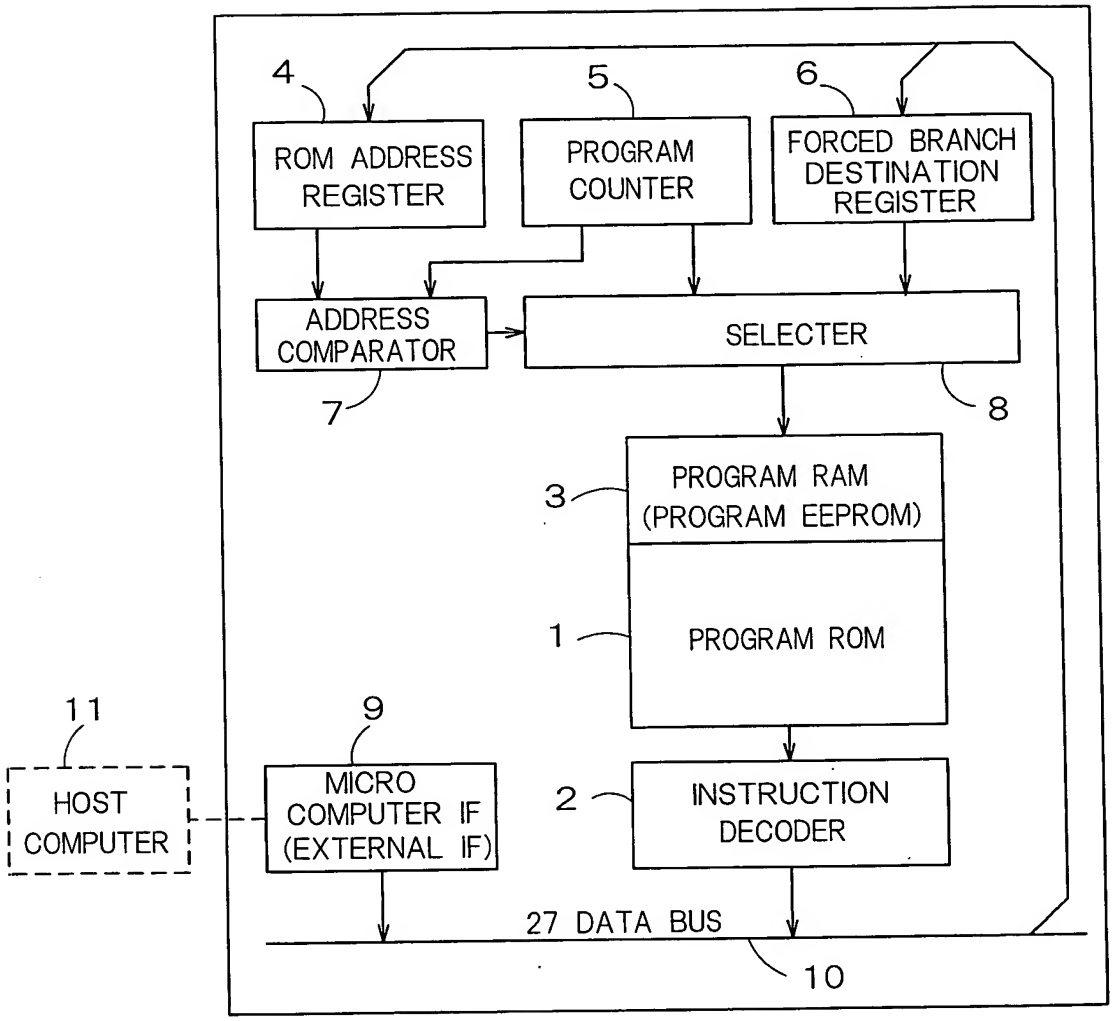
4
5
6
ROM ADDRESS REGISTER
PROGRAM COUNTER
FORCED BRANCH DESTINATION REGISTER
ADDRESS COMPARATOR
SELECTER
7
8
3
PROGRAM RAM (PROGRAM EEPROM)
1
PROGRAM ROM
11
9
HOST COMPUTER
MICRO COMPUTER IF (EXTERNAL IF)
2
INSTRUCTION DECODER
27 DATA BUS
10

FIG. 1

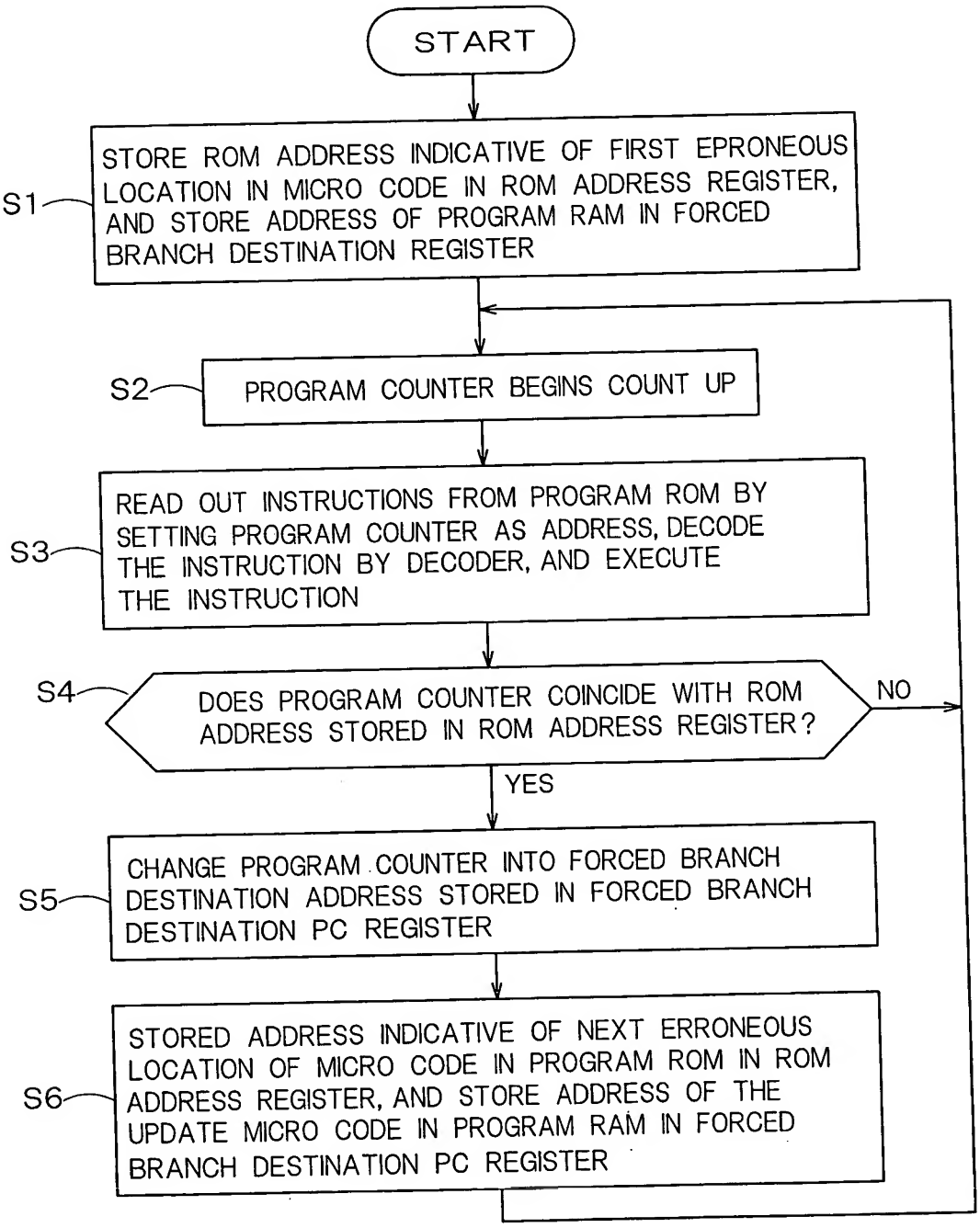
START
S1
STORE ROM ADDRESS INDICATIVE OF FIRST EPRONEOUS LOCATION IN MICRO CODE IN ROM ADDRESS REGISTER, AND STORE ADDRESS OF PROGRAM RAM IN FORCED BRANCH DESTINATION REGISTER
S2
PROGRAM COUNTER BEGINS COUNT UP
S3
READ OUT INSTRUCTIONS FROM PROGRAM ROM BY SETTING PROGRAM COUNTER AS ADDRESS, DECODE THE INSTRUCTION BY DECODER, AND EXECUTE THE INSTRUCTION
S4
DOES PROGRAM COUNTER COINCIDE WITH ROM ADDRESS STORED IN ROM ADDRESS REGISTER?
NO
YES
S5
CHANGE PROGRAM COUNTER INTO FORCED BRANCH DESTINATION ADDRESS STORED IN FORCED BRANCH DESTINATION PC REGISTER
S6
STORED ADDRESS INDICATIVE OF NEXT ERRONEOUS LOCATION OF MICRO CODE IN PROGRAM ROM IN ROM ADDRESS REGISTER, AND STORE ADDRESS OF THE UPDATE MICRO CODE IN PROGRAM RAM IN FORCED BRANCH DESTINATION PC REGISTER

FIG. 2

```
000   move   ROM_ADR, #h100
001   move   BRANCH DESTINATION reg, #h010
002   SET FORCED BRANCH TO ENABLE
003   JUMP   h080
... (OMISSION) ...
010   move   ROM_ADR, #h200
011   move   BRANCH DESTINATION reg, #h110
012   JUMP   h120
... (OMISSION) ...
030   move   ROM_ADR, #h300
031   move   BRANCH DESTINATION reg, #h210
033   JUMP   h140
```

FIG. 3

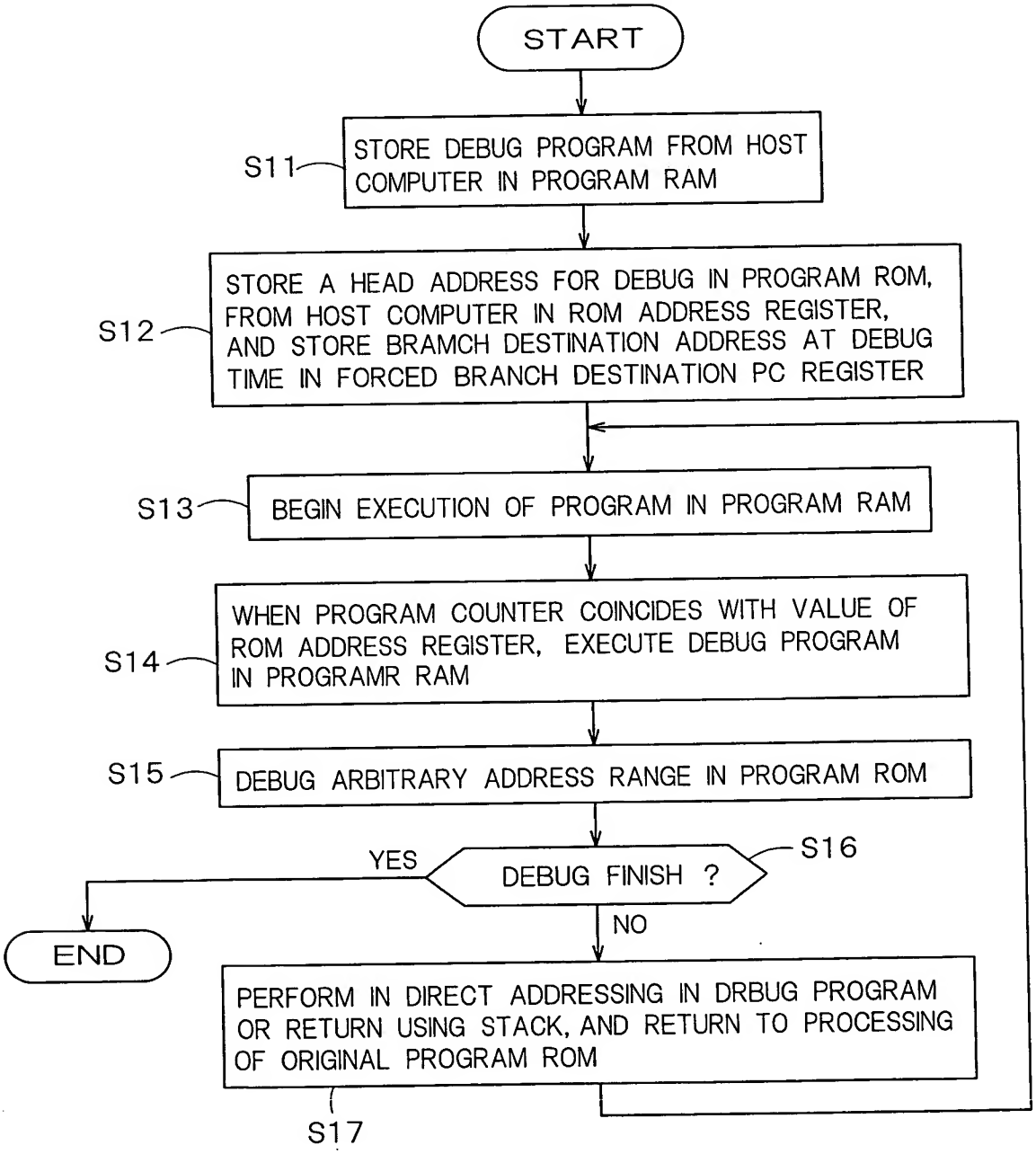
START
S11
STORE DEBUG PROGRAM FROM HOST COMPUTER IN PROGRAM RAM
S12
STORE A HEAD ADDRESS FOR DEBUG IN PROGRAM ROM, FROM HOST COMPUTER IN ROM ADDRESS REGISTER, AND STORE BRAMCH DESTINATION ADDRESS AT DEBUG TIME IN FORCED BRANCH DESTINATION PC REGISTER
S13
BEGIN EXECUTION OF PROGRAM IN PROGRAM RAM
S14
WHEN PROGRAM COUNTER COINCIDES WITH VALUE OF ROM ADDRESS REGISTER, EXECUTE DEBUG PROGRAM IN PROGRAMR RAM
S15
DEBUG ARBITRARY ADDRESS RANGE IN PROGRAM ROM
S16
DEBUG FINISH ?
YES
NO
END
PERFORM IN DIRECT ADDRESSING IN DRBUG PROGRAM OR RETURN USING STACK, AND RETURN TO PROCESSING OF ORIGINAL PROGRAM ROM
S17

FIG. 4